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(54) **DISCRIMINATION TIMING CONTROL CIRCUIT.**

(57) A circuit for controlling the discrimination timing so that it is best adapted for discriminating a multi-value signal. The gradient of a multi-value signal is discriminated at a central discrimination moment from the discrimination data at at least three consecutive discrimination moments, lag in the discrimination timing is determined from the gradient and an error signal at the central discrimination moment, and the timing is so controlled that the shift in the phase of the discrimination clocks decreases. Further, it is made possible to perform two kinds of gradient discrimination, and the gradient discrimination is effected alternatively depending upon the condition of the circuit.

EYE PATTERN AND DICISION WAY

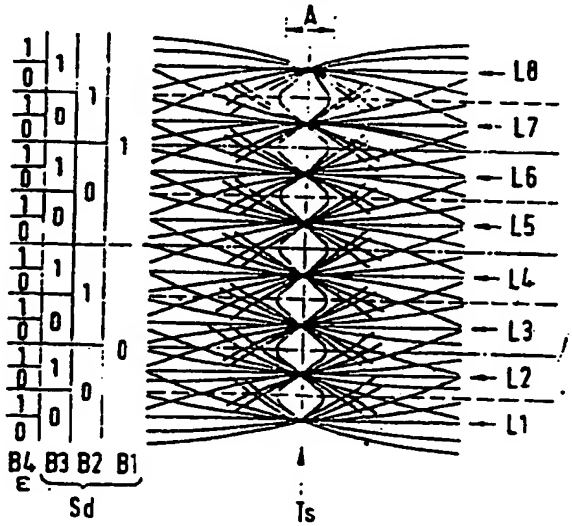

Fig. 2

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DECISION TIMING CONTROL CIRCUIT

TECHNICAL FIELD

The present invention relates to a decision timing control circuit provided in the receiving side of the radio data transmission system utilizing the multi-level amplitude modulation method.

BACKGROUND ART

In the radio data transmission system utilizing the multi-level amplitude modulation, for instance, the 64-level quadrature amplitude modulation (QAM), binary transmission data is distributed to 3 bits for I channel and 3 bits for Q channel in the sending side. The 3 bits of respective channels are subjected to D/A conversion in the timing of predetermined clock and these signals converted to 8-level signals both in the I channel and Q channel. The 8-level signals of I and Q channels are respectively transmitted after the quadrature amplitude modulation.

A constitution of the receiving side is indicated

in Fig. 1.

A demodulator 10 inputs a receiving signal S_{in} from a receiver (not illustrated) and outputs the 8-level signals S_{ai}, S_{aq} of I and Q channels. The 8-level signals S_{ai}, S_{aq} of both I and Q channels are respectively input to data recovery circuits 20, 30 of I and Q channels and the I channel signal is also input to a bit timing recovery circuit (BTR) 40. The bit timing recovery circuit 40 rectifies the 8-level signal S_{ai} of I channel with a full-wave rectifier 41 to generate the clock element. The full-wave rectified signal is then input to a phase comparator 43 together with an output of a voltage controlled oscillator (VCO) 42. A phase difference signal output from the phase comparator 43 is applied as a control voltage to VCO 42 through a low-pass filter 44. Thereby, VCO 42 outputs the clock signal CLK which is synchronized with the 8-level signal S_{ai} of I channel.

Meanwhile, the data recovery circuit 20 of I channel inputs the 8-level signal S_{ai} of I channel to the A/D converter 22 provided as a decision circuit through an equalizer 21. The A/D converter 22 inputs the clock CLK sent from the bit timing recovery circuit 40 through a variable phase shifter 23, decides the

8-level signal S_{ai} of I channel input in the timing of clock CLK and converts it into a binary digital signal, and outputs the 1 bit lower than the upper 3 bits as the decision error signal ε with such upper 3 bits used as the decision data S_d.

Moreover, the data recovery circuit 30 of Q channel has the structure similar to that of the data recovery circuit 20 of I channel.

For the radio communication system, it is necessary to limit the frequency band of sending signal and therefore a filter is used in the sending side. Accordingly, the 8-level signal demodulated in the receiving side has the gentle waveform in place of the rectangular waveform. As a result, the 8-level signal demodulated has the eye patter indicated in Fig. 2 and the eye aperture A is rather narrow.

As the decision timing deviates from the center of such aperture A, the error rate becomes worse. Therefore, the phase of recovered clock is adjusted manually with the variable phase shifter and it is fixed when decision is carried out at the optimum decision timing T_s.

However, here lies a problem that it is likely that the clock phase deviates, even after it is once

fixed, from the optimum decision timing due to temperature change or voltage variation and it is difficult to quickly match the clock phase and optimum decision timing during the pulling-in period in the initial stage of data transmission or when intersymbol interference due to the fading sometimes appearing increases.

In addition, there rises a problem that the demodulated multi-level signal S_{ai} (S_{aq}) is disturbed during pulling-in period or when intersymbol interference increases, a number of credible signal points which are required to control synchronization between clock phase and optimum decision timing is a little and thereby a longer time is required until the end of control for matching.

Furthermore, it is also a problem that adjustment of equalizer 20 makes complicated and large scale hardware structure of equalizer.

In order to solve such problems, a decision timing control circuit indicated in the Japanese Patent Application No. 141856/1986 has been proposed. However, since this decision timing control circuit monitors information corresponding to an error rate and controls the phase of clock to reduce such information, the

direction of phase shift is not determined directly from the decision digital signal and phase shift direction is determined by "Trial and Error".

Therefore, such control is complicated and easily receives influences of line conditions.

DISCLOSURE OF THE INVENTION

It is a first object of the present invention to provide a circuit which automatically controls the decision timing in the receiving side of the radio data transmission system, considering the problems of prior art explained above. It is a second object of the present invention to provide a decision timing control circuit which assures quick and accurate synchronization of timing even under the conditions other than the normal condition, for instance, during the pulling-in condition or when intersymbol interference increases. It is a third object of the present invention to provide a decision timing control circuit to directly obtain information about the deviating direction of timing from the data decided. Moreover, it is a fourth object of the present invention to provide a decision timing control circuit which may be formed by a simple circuit structure.

In view of attaining the objects explained above, the present invention controls decision timing by deciding slope of multi-level signal at the center decision timing T_0 from the decision data S_{d-}, S_{d0}, S_{d+} in at least three continuous decision timings T_{-1}, T_0, T_{+1} and deciding deviation of decision timing from such slope and error signal ε of decision timing T_0. Thereby, adequate decision of slope is carried out respectively when the line condition is normal and deteriorated. Under the normal condition, the slope can be decided from the monotonous increase or decrease, and when the line condition is deteriorated, the slope can be decided depending on high or low level of decided data before and after the demodulated multi-level signal which is higher than the highest decision level or is lower than the lowest decision level.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram indicating the structure of the receiving side of the prior art;

Fig. 2 indicates an eye pattern and decision way;

Fig. 3 is a basic block diagram of the present invention;

Fig. 4 indicates an example of slope decision in the present invention;

Fig. 5 indicates relationship between slope, deviation of decision timing and decision error signal;

Fig. 6 is a block diagram of a first embodiment of the present invention;

Fig. 7 indicates another exmaple of slope discrimination in the present invention;

Fig. 8 is a block diagram of a second embodiment of the present invention;

Fig. 9 is a block diagram of a third embodiment of the present invention;

Fig. 10 is a basic block diagram of a fourth embodiment of the present invention; and

Fig. 11 is a detail block diagram of the fourth embodiment of the present invention.

BASIC CONSTITUTION OF THE PRESENT INVENTION

Fig. 3 indicates the basic constitution of the present invention.

The decision circuit 50 inputs a multi-level signal S_a and outputs decision data S_d and decision error signal ε. When a number of levels of multi-

level signal is determined as 2^n, the decision data S_d becomes a binary digital signal of n bits. The decision error signal indicates that the input multi-level signal corresponds to the upper or lower range than the center in the range decided in each level. For example, in the case of 8-level signal, three bits B1 ~ B3 indicate to which level in the 8 levels (L1 ~ L8) the input signal is near as indicated in Fig. 2 and one bit B4 lower than the decision data is output as the decision error signal ε.

The slope decision means 60 decides slope of multi-level signal at the center decision timings from the decision data of at least continuous three decision timings and outputs a slope indication signal (γ) which indicates such slope is positive or negative. For instance, as indicated in Fig. 4, in case the levels indicated by the decision data at the continuous three decision timings T_{-1}, T_0, T_{+1} increase monotonously like the line (a), the slope at the decision timing T_0 is positive. Moreover, the levels decrease monotonously like the line (b), the slope at the decision timing T_0 is negative. But, in case the levels are once decreased and thereafter increased, the slope cannot be defined and becomes unclear.

A lead/delay decision means 70 decides whether the decision timing of decision circuit 50 is leading or delayed from the optimum decision timing T_s from the slope indication signal and decision error signal ε at the center decision timing and outputs a phase decision signal P. For instance, in the case of positive slope indicated by a solid line in Fig. 5, the decision error signal becomes 0 when the decision timing by the clock CLK is leading the optimum decision timing T_s or becomes 1 when it is delayed. On the other hand, in case the slope is negative as indicated by a broken line, relationship between the lead and delay of decision timing and 1, 0 of the decision error signal ε is reversed from that of positive slope. Thereby, lead or delay of the decision timing can be decided from positive or negative slope and decision error signal ε.

A clock generating means 80 generates the clock for decision to send it to the decision circuit 50 and changes phase of clock on the basis of the phase decision signal P sent from the lead/delay decision means 70.

First Embodiment:

A structure of the first embodiment of the present invention is indicated in Fig. 6.

The A/D converter 51 is corresponding to the decision circuit 50 of Fig. 3 and inputs the 8-level signal S_a and outputs the decision data S_d and decision error signal ε indicated in Fig. 2.

The delay circuits 61, 62 and ROM 63 correspond to the slope decision means 60 of Fig. 3 and the decision data S_d is sequentially input to the cascaded delay circuits (T) 61 and 62.

As a delay circuit, a D type flip-flop may be used. When the decision data output from the delay circuit 61 is the decision data S_{d0} at the center decision timing, the decision data S_{d-} which has appeared before one clock is output from the delay circuit 62 and the decision data S_{d+} which appears after one clock is input to the delay circuit 61. These three decision data S_{d-}, S_{d0}, S_{d+} are input to ROM 63 as the adresses. In the case of 8-level signal, the address of ROM 63 becomes 9 bits since the decision data is formed by 3 bits. Contents of X and Y of ROM 63 are respectively slope polarity signal γ_1 of one bit and validity signal γ_2 of one bit. These slope polarity signal γ_1 and validity signal γ_2 correspond to the slope indication signal γ. The slope polarity signal γ_1 becomes "1" for positive slope or "0" for negative slope. The validity

display signal γ_2 becomes "1" when the slope polarity sigal γ_1 is valid or "0" when it is invalid. For example, in the case of curve (a) of Fig. 4, S_{d-} becomes "100", S_{d0} becomes "101" and S_{d+} becomes "110" and the slope is positive. Therefore, contents X, Y of address "100101110" of ROM 63 respectively become "1", "1". In similar, contents X, Y of address "101011001" for the line (b) become "0", "1" and contents X, Y of address "011001100" for the line (c) become "0" or "1" and "0". When Y = "0", content of X may be "0" or "1" since it does not give any influence on the succeeding circuits. For the other addresses, X = "1", Y = "1" can be obtained for monotonous increase, while X = "0", Y = "1" for monotonous decrease and X = "0" or "1", Y = "0" for the slopes other than monotonous increase and monotonous decrease.

An exclusive OR circuit 71, delay circuit (T) 72, AND circuit 73 and D type flip-flop (FF) 74 correspond to the lead/delay decision means 70 of Fig. 3. The slope polarity signal γ_1 sent from ROM63 is input to the one input terminal of exclusive OR circuit 71, while the decision error signal ε is input to the other input terminal through the delay circuit 72. The delay circuit 72 is provided to synchronize the decision

error error signal ε to the timing of inputting the decision data S_{d0} at the center decision timing to ROM 63. An output of the exclusive OR circuit 71 becomes "0" which indicates that the decision timing is delayed when the slope polarity signal γ_1 is "0" and decision error signal ε is "0" and when the slope polarity signal γ_1 is "1" and decision error signal ε is "1" and becomes "1" which indicates that the decision timing is leading in other cases. Meanwhile, the validity signal γ_2 is converted to the RZ (Return to Zero) signal by the AND circuit 70 and is then input to the clock terminal C of D type flip-flop. Thereby, an output of the exclusive OR circuit 71 is newly held in the D type flip-flop 74 when the validity signal is "1". If the validity signal γ_2 is "0", the old value is still held. The value held in the D type flip-flop 74 is output as the phase decision signal P.

A bit timing recovery circuit 81, integrator 82 and phase shifter 83 correspond to a clock generating means 80. The clock recovery circuit 81 is similar to the bit timing recovery circuit (BTR) 40 indicated in Fig. 1 and recovers the clock from the 8-level signal S_a to output it. The integrator 82 integrates the phase decision signal P. The phase shifter 83 shifts

the recovered clocks depending on the integral value and outputs it to the A/D converter 51 as the decision clock CLK. Thereby, the clock CLK is controlled in such a manner as the decision is always carried out in the optimum decision timing.

Second Embodiment:

In realization of the slope decision indicated in Fig. 4, if line condition is bad and decision of the center decision timing T_0 is conducted at the next level, the decision error signal has reverse polarity and decision timing control error may be generated.

Fig. 7 indicates an example of slope decision which is suitable for bad line condition. When the 8-level signal changes as the line I indicates, namely, when the level of decision data at the decision timing T_{-1} is lower than the center level L_c, the level of decision data at the decision timing T_0 is maximum level L8 and the level of decision data at the decision timing T_{+1} is higher than the center level L_c, it is impossible that the signal to be decided in the level higher than that at the decision level T_0 is decided in the level lower than the actual level. Therefore, when the decision error signal ε is "1", such information has high reliability and it is also reliable that slope

is positive. As explained above, when the level of decision data at the decision timing T_0 is maximum level and the decision error signal $\mathcal{E}$ is "1" and when the level of decision data at the decision timing T_0 is minimum level and the decision error signal $\mathcal{E}$ is "0", the decision error signal $\mathcal{E}$ has high reliability. When the level of decision data at the decision timing T_{-1} and the level of decision data at the decision timing T_{+1} are opposed to each other around the center level L_c, it is very much reliable to make decision for positive or negative slope at the decision timing T_0. Namely, the decision error signal $\mathcal{E}$ has very high reliability when the decision error signal $\mathcal{E}$ is "1" in the waveform in such a type as indicated by the line I or II in Fig. 7 and when the decision error signal $\mathcal{E}$ is "0" in the waveform in such a type as indicated by the line III or IV, and moreover the waveform indicated by the line I or III has high reliability of positive slope, while the waveform indicated by the line II or IV has high reliability of negative slope.

Fig. 8 indicates a constitution of the second embodiment of the present invention.

As a decision circuit 50, lead/delay decision

means 70 and clock generating means 80, the circuits indicated in Fig. 6 may be used.

The delay means 61, 62, 65, ROM 64, inverse exlcusive OR circuit 66 and OR circuit 67 correspond to the slope decision means 60 of Fig. 3 and conduct slope decision indicated in Fig. 7. Operations of delay circuits 62 and 62 are same as those of Fig. 6. As the contents X of ROM64, the slope polarity signal γ_1 is written, while the data "1" is written in the address corresponding to the type of lines II and IV and the data "0" in the address corresponding to the type of lines II and IV. As the contents Y of ROM64, the data "1" is written in the address corresponding to the type of lines I, II, III and IV and the data "0" in the other addresses. The content Z indicates that the decision data at the decision timing T_0 corresponds to the maximum level or minimum level, and the data "1" is written in the address corresponding to the type of lines I and II, while the data "0" in the address corresponding to the type of lines III and IV. The Z output of ROM64 and the decision error signal ε at the decision timing T_0 sent through the delay circuit 65 are input the inverse exclusive OR circuit 66. The exclusive NOR circuit 66 outputs "1" when the Z output

of ROM64 is "1" and the decision error signal $\mathcal{E}$ is "1", and when the Z output of ROM64 is "0" and the decision error signal $\mathcal{E}$ is "0" and also outputs "0" in other cases. Both outputs of exclusive NOR circuit 66 and Y output of ROM64 are input to the AND circuit 67. Thereby, an output of the AND circuit 67 becomes "1" for the type indicated by lines I and II and for the decision error signal $\mathcal{E}$ of "1" and becomes "0" for other cases. Accordingly, an output of the AND circuit 67 may be used as the validity signal γ_2. Moreover, the X output of ROM64 may be used as the slope polarity signal γ_1.

Third Embodiment:

In the clock recovery circuit 81 of the embodiment indicated in Fig. 6, VCO 42 controls the oscillation frequency (phase) based on the phase difference signal sent from a phase comparator 43 as indicated in Fig. 1. An output of VCO 42 is further phase-controlled by the phase shifter 83 of Fig. 6. Therefore, the phase control is carried out at the two points for the clock CLK and this circuit structure is not effective.

Fig. 9 is the structure of the third embodiment. As the decision circuit 50, slope decision means 60 and lead/delay decision means 70, the circuits indicated in

Fig. 6 may be used.

The integrator 84 and VCO85 corresponds to a clock generating means 80 indicated in Fig. 6. The integrator 84 integrates the decision signal P sent from the lead/delay decision means 70. VCO85 oscillates with he frequency corresponding to an integral value and outputs the decision clock CLK to the decision circuit 50. The integrator 84 operates in common as the integrator 82 of Fig. 6 and the low-pass filter 44 of Fig. 1. Thereby, the full-wave rectifier 41 and phase comparator 43 of Fig. 1 and the phase shifter 83 of Fig. 6 may be omitted.

Fourth Embodiment:

Fig. 10 is a basic constitution of the fourth embodiment of the present invention. In Fig. 10, a line condition decision means 90 is provided in addition to the constitution indicated in Fig. 3 in this embodiment and the first slope decision means 60_{-1} and the second slope decision means 60_{-2} are provided as the slope decision means 60 to select the one of these slope decision means 60_{-1}, 60_{-2} in accordance with the line condition. As the decision circuit 50, lead/delay decision means 70 and clock generating means 80, the circuits similar to those of Fig. 6 may be used.

Fig. 11 indicates detail constitution of the fourth embodiment of the present invention. The internal constitution of the slope decision means 60_{-1} of Fig. 1 and that of the slope decision means 60_{-2} of Fig. 2 are respectively similar to that of the slope decision means 60 of Fig. 8. However, ROM63 and ROM64 are respectively provided with the enable terminals ($\overline{EN}$, EN) and these are driven when "0" and "1" are respectively input to these terminals. These circuits stop the operations when "1" and "0" are respectively input to such terminals. Moreover, the delay circuits 61 and 62 are used in common by the first and second slope decision means 60_{-1}, 60_{-2}.

The exclusive NOR circuit 91, integrator 92 and comparator 93 correspond to the line condition decision means 90 of Fig. 10.

The A/D converter 52 corresponds to the decision circuit 50 of Fig. 3 and outputs not only the decision data S_d and decision error signal but also the sub-decision error signal ε'. The sub-decision error signal ε' indicates whether the multi-level signal exists in the upper or lower range when the range sectioned by the decision error signal ε is further divided into two sections, and the signal becomes "1"

and "0" for respective ranges. Such signal can be obtained as the 5th bit B5 for decision circuit of the 8-level signal.

When the decision error signal ε is "1" and the sub-decision error signal ε' is "1", the input level to the A/D converter 52 is in the higher range among two ranges having the levels higher than the correct decision level. In similar, when the decision error signal ε is "0" and sub-decision error signal ε' is "0", an error from the correct decision level is large. On the other hand, when the decision signal and sub-decision error signal ε' are respectively "1" and "0" or "0" and "1", an error from the correct decision level is small.

The exclusive NOR circuit 91 outputs "1" when the decision error signal ε and sub-decision error signal ε' are respectively "0" and "0" or "1" and "1", namely when error from the correct decision level is large, and also outputs "0" when the decision error signal and sub-decision error signal ε' and sub-decision error signal are respectively "0" and "1" or "1" and "0", namely when error from the correct decision level is small.

An integrator 92 integrates output "1" of the exclusive NOR circuit 91 with the predetermined time

constant. The comparator 93 compares such integrated value with the reference voltage V_r and outputs "1" when the integrated value is larger or "0" when the integrated value is smaller. That is, when the error from the correct decision level often becomes large, the integrator decides that the line condition has changed bad and outputs "1".

While the comparator 93 outputs "0", ROM63 of the first slope decision circuit 60_{-1} is driven to realize the slope decision explained in regard to the first embodiment and outputs the slope polarity signal γ_1 and validity signal γ_2 respectively through the OR circuits 68 and 69. In this case, the probability for input of the waveform which makes valid the slope polarity signal becomes high comparatively.

While the comparator 93 outputs "1", ROM64 of the second slope decision circuit 60_{-2} is driven to realize the slope decision explained in regard to the second embodiment and outputs the slope polarity signal γ_1 and validty signal γ_2 respectively through the OR circuits 68 and 69. In this case, the probability for input of waveform which makes valid the slope polarity signal is low but reliability of slope decision when it becomes valid is high and large effect can be obtained when the

line condition becomes bad.

In each embodiment explained above, the slope decision is carried out on the basis of the decision data of three continuous decision timings but it may also be done on the bais of the decision data of three or more decision timings.

CLAIMS:

1. A decision timing control circuit, in the radio data transmission system wherein the sending side transmits the signal through multi-level amplitude modulation of send data with the carrier while the receiving side obtains the send data by deciding the multi-level signal demodulated with a decision circuit which also outputs a decision error sigal (£) indicating whether the demodulated multi-level signal is higher or lower than the correct decision level in addition to such send data (S_d) decided in the timing of recovered clock, comprising:

a slope decision means (60) which is operatively connected with the decision circuit (50) and outputs a slope indication signal (£) which decides slope of multi-level signal at the center decision timing on the basis of the decision result (S_d) in at least three continuous decision timings and indicates whether slope is positive or negative,

a lead/delay decision means (70) which is operatively connected with the decision circuit (50) and slope decision means (60) and outputs the phase decision signal (P) by deciding whether the decision timing at the decision point is leading or delayed from

the decision error signal (ε) at the center decision timings and the decided slope (γ), and

a clock generation means (80) which is operatively connected with the lead/delay decision means (70) and the decision circuit (50) and generates the phase-controlled clock (CLK) based on the the phase decision signal (P) to be sent to the decision circuit (50).

2. A decision timing control circuit according to claim 1, wherein the slope decision means (60) outputs, as the slope indication signal (γ), the slope polarity signal (γ_1) which indicates the positive slope when the decision data (S_d) of decision circuit (50) increases monotonously or the negative slope when it decreases monotonously and the validity signal (γ_2) which indicates validity of slope polarity signal when the decision data (S_d) increases or decreases monotonously or invalidity of slope polarity signal when it does not increase or decrease monotonously.

3. A decision timing control circuit according to claim 1, wherein the slope decision means (60) outputs, as the slope indication signal (γ), the validity signal (γ_2) which indicates validity when the

decision data (S_{d0}) at the center decision timing (T_0) in the decision circuit (50) has the maximum or minimum level, the decision data (S_{d-}) at the preceding decision timing (T_{-1}) and the decision data (S_{d+}) of the succeeding decision timing (T_{+1}) have the levels opposed to each other around the center level and the error bit ($\mathcal{E}$) higher than the maximum level or lower than the minimum level, or indicates invalidity in other cases and the slope polarity signal (γ_1) which indicates the positive slope when the decision data (S_{d+}) at the succeeding decision timing (T_{+1}) is higher than the decision data (S_{d-}) at the preceding decision timing (T_{-1}) in case the validity signal (γ_2) indicates the validity or indicates the negative slope when the decision data (S_{d+}) at the succeeding decision timing (T_{+1}) is lower than the decision data (S_{d-}) at the preceding decision timing (T_{-1}).

4. A decision timing control circuit according to any of the claims 1 to 3, further comprising a line condition decision means (90) which is operatively connected with the slope decision means (60) and decides line condition to output the decision result to the slope decision means (60), wherein the slope decision

means (60) comprises a first slope decision means (60_{-1}) and a second slope decision means (60_{-2}) any one of which is selectively driven in accordance with the decision result of line condition.

5. A decision timing control circuit according to any of the claims 1 to 4, wherein the lead/delay decision means (70) decides lead or delay of decision timing from exclusive OR between the decision error signal ($\mathcal{E}$) sent from the decision circuit (50) and the slope polarity signal (γ_1) sent from the slope decision means (60) and holds the decision result as a new decision result when the validity signal (γ_2) sent from the slope decision means (60) indicates validity or holds the old decision result as it is when the validity signal (γ_2) indicates invalidity.

6. A decision timing control circuit according to any of the claims 1 to 5, wherein said clock generation means (80) comprises a bit timing recovery circuit (81) which recovers the clock from multi-level signal, a integrator (82) which integrates the phase decision signal (P) and a phase shifter (83) which shifts phase of clock recovered on the basis of the integrated value to output to the decision circuit (50).

7. A decision timing control circuit according to any of the claims 1 to 5, wherein the clock generation means (80) comprises a integrator (84) which integrates the phase decision signal (P) and an oscillator (85) which oscillates with the frequency corresponding to the integrated value.

Fig. 1

BLOCK DIAGRAM OF CONSTITUTION IN RECEIVING SIDE OF PRIOR ART

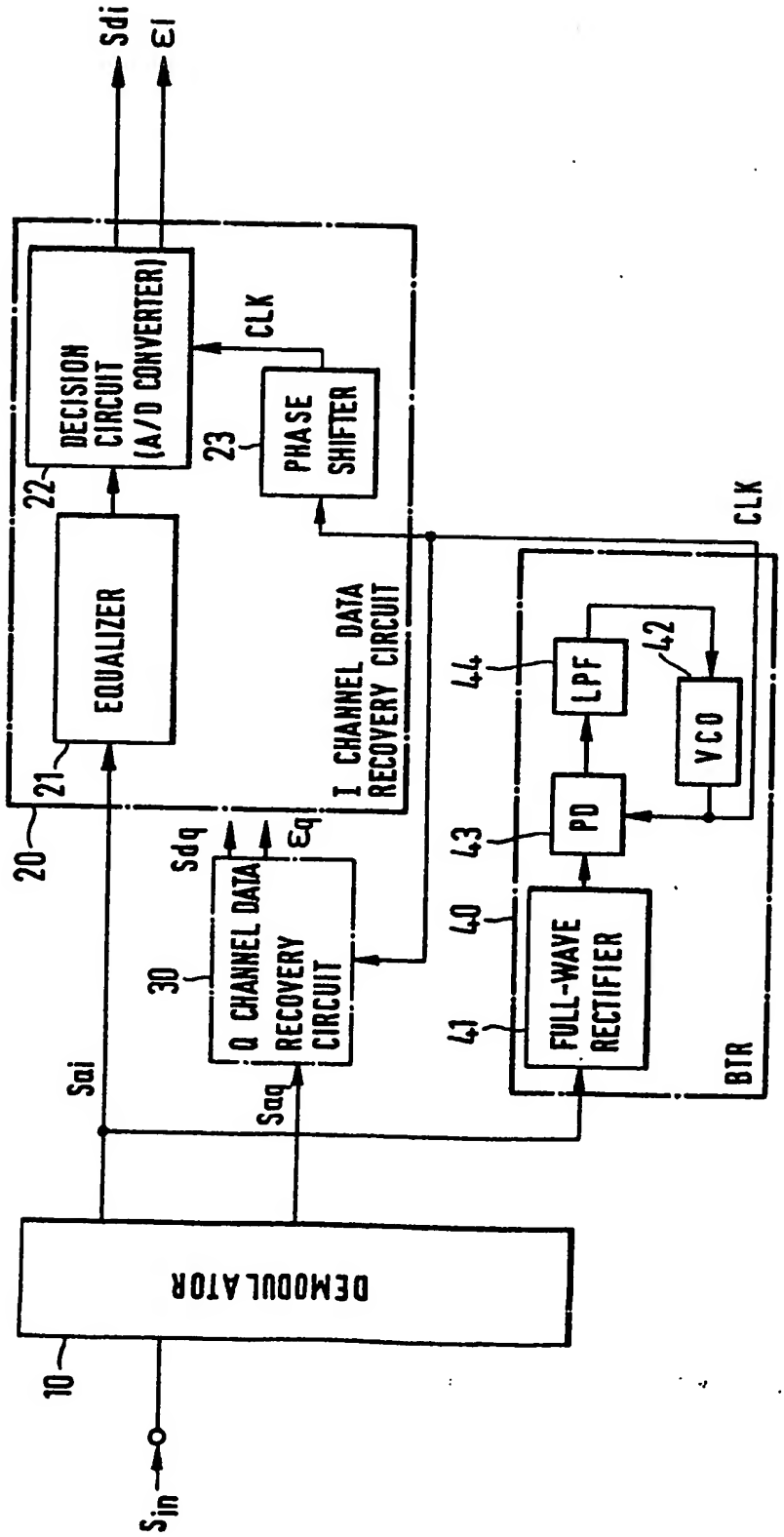


Fig.2
EYE PATTERN AND DICISION WAY

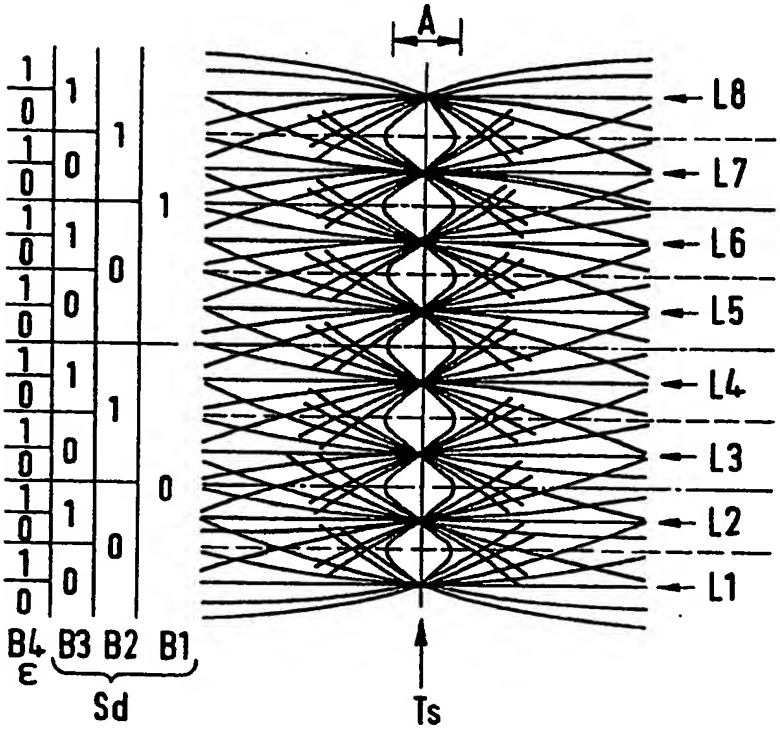


Fig.3
BASIC BLOCK DIAGRAM OF PRESENT INVENTION

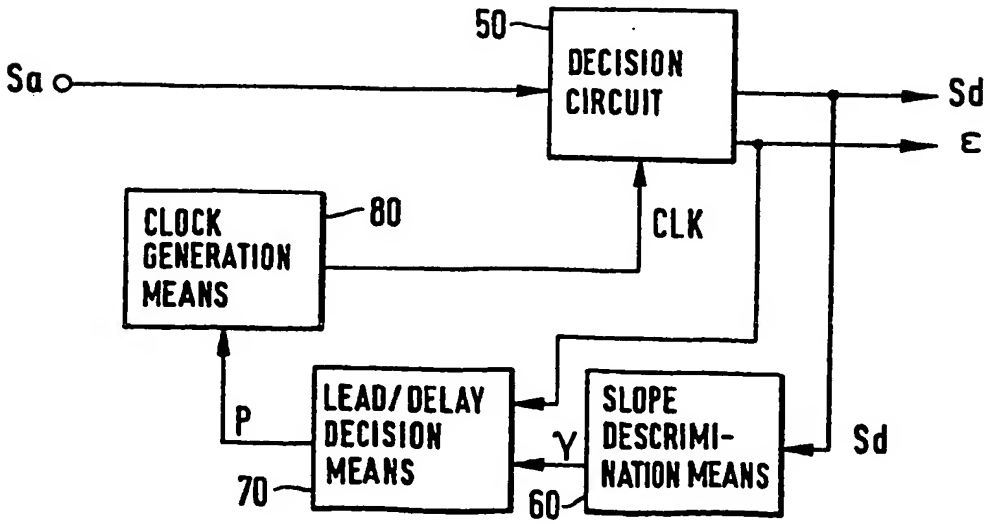


Fig. 4

EXAMPLE OF SLOPE DISCRIMINATION IN PRESENT INVENTION

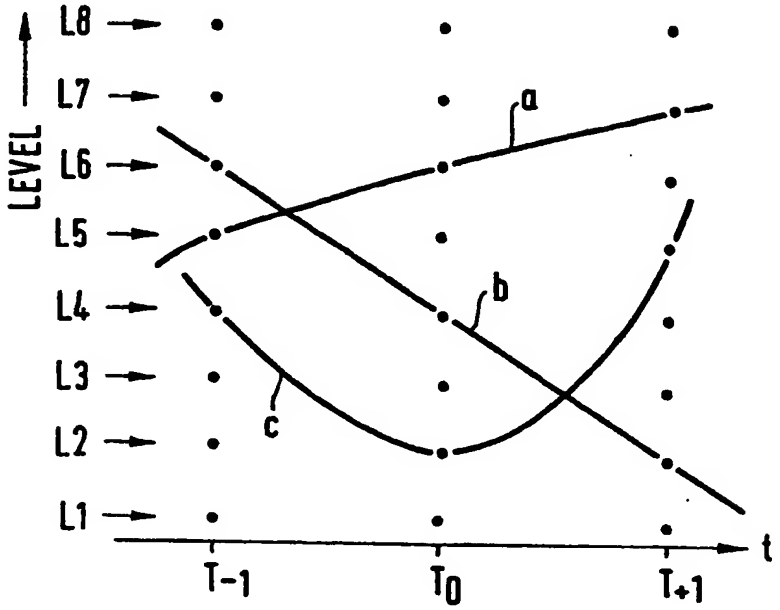
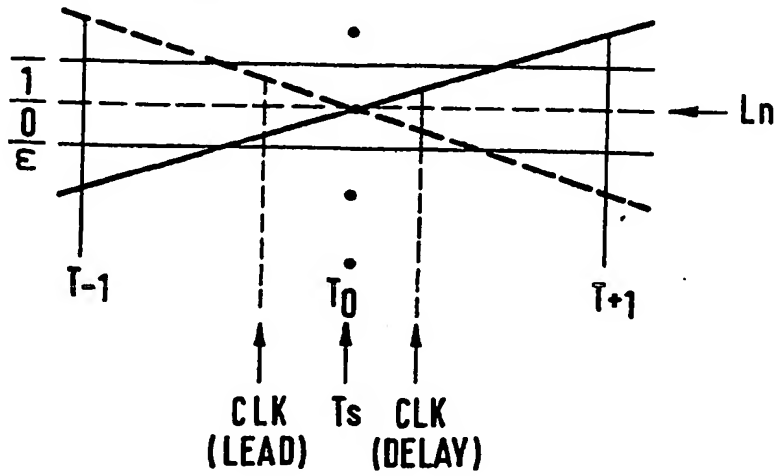


Fig. 5

DIAGRAM INDICATING RELATIONSHIP BETWEEN SLOPE, DEVIATION OF DECISION TIMING AND DECISION ERROR SIGNAL



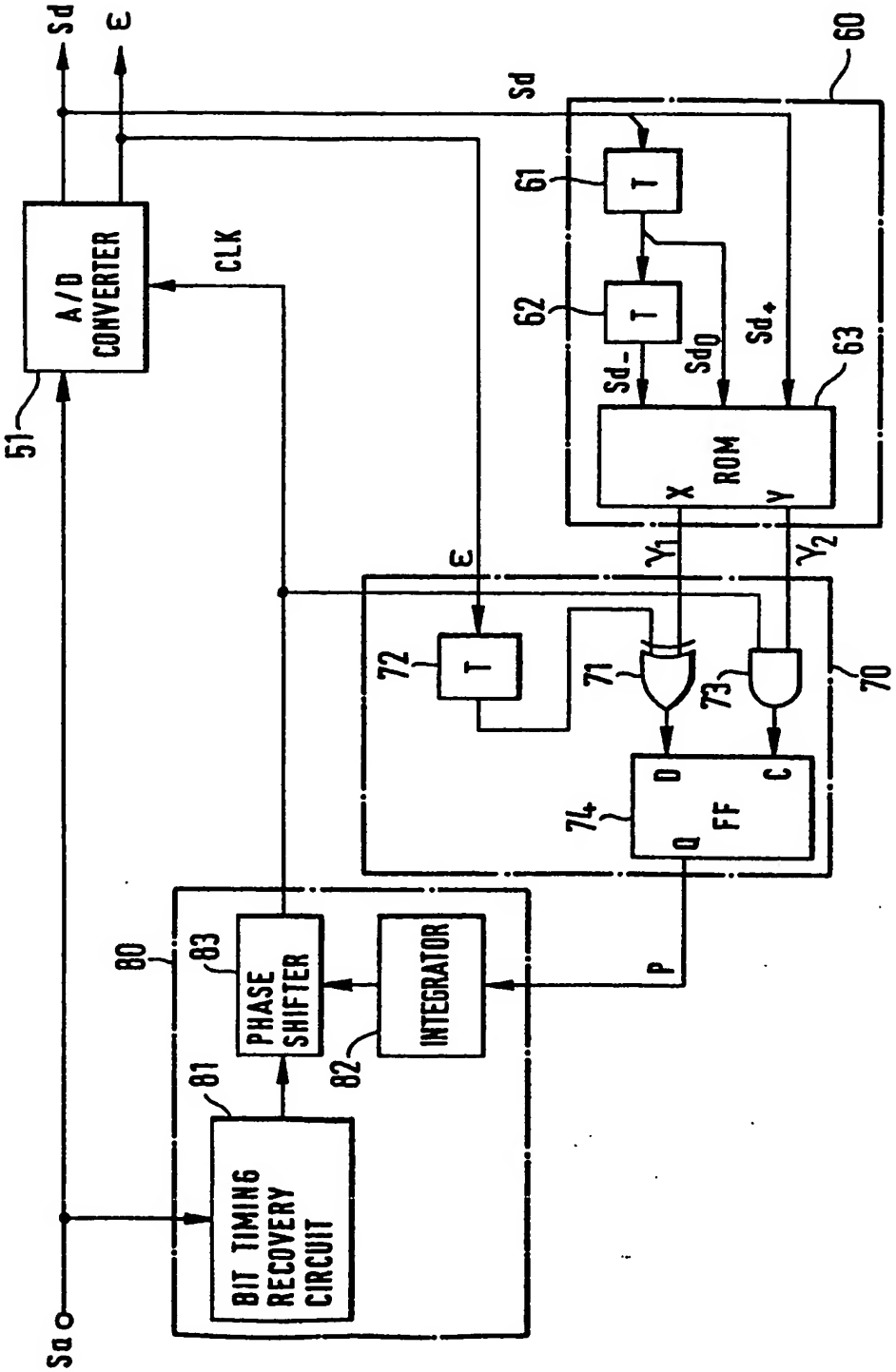


Fig.6
BLOCK DIAGRAM OF FIRST EMBODIMENT OF PRESENT INVENTION

Fig.7

ANOTHER EXAMPLE OF SLOPE DISCRIMINATION IN PRESENT INVENTION

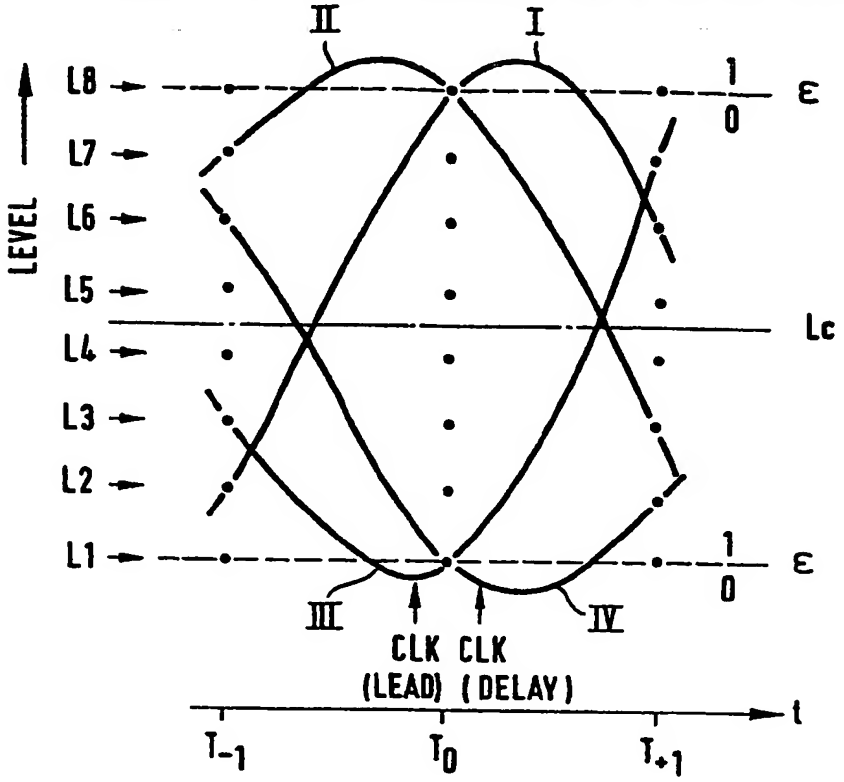


Fig.8

BLOCK DIAGRAM OF SECOND EMBODIMENT OF PRESENT INVENTION

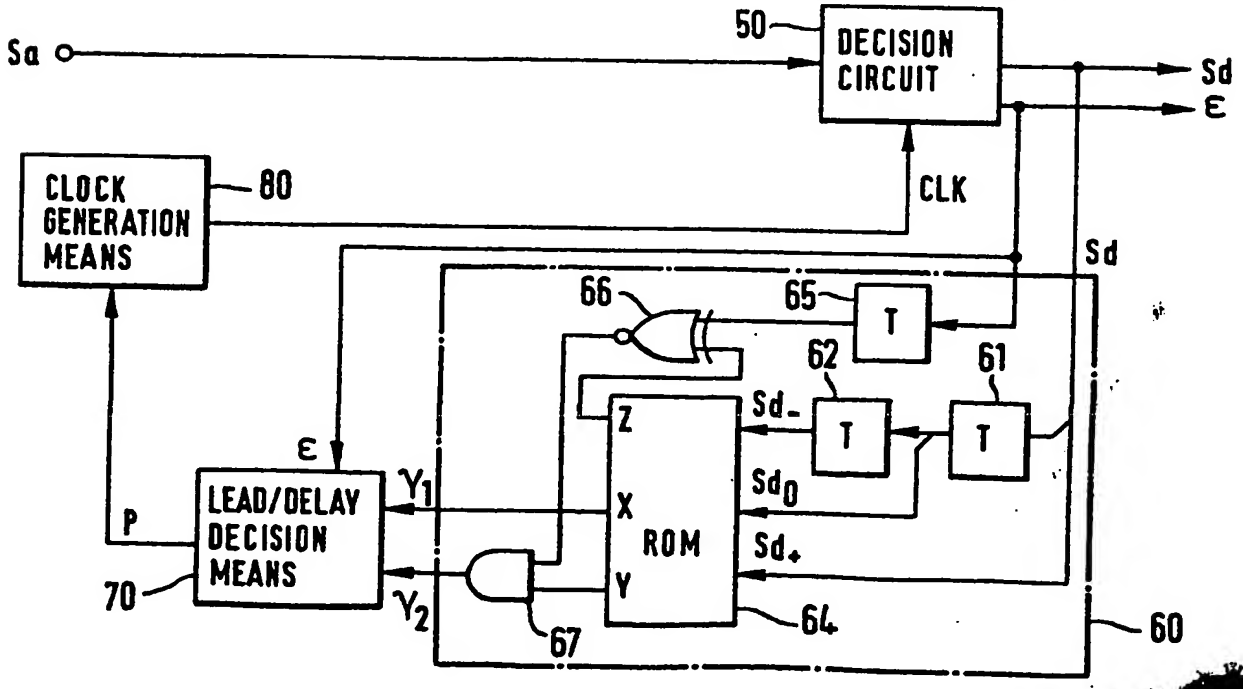


Fig.9

BLOCK DIAGRAM OF THIRD EMBODIMENT OF PRESENT INVENTION

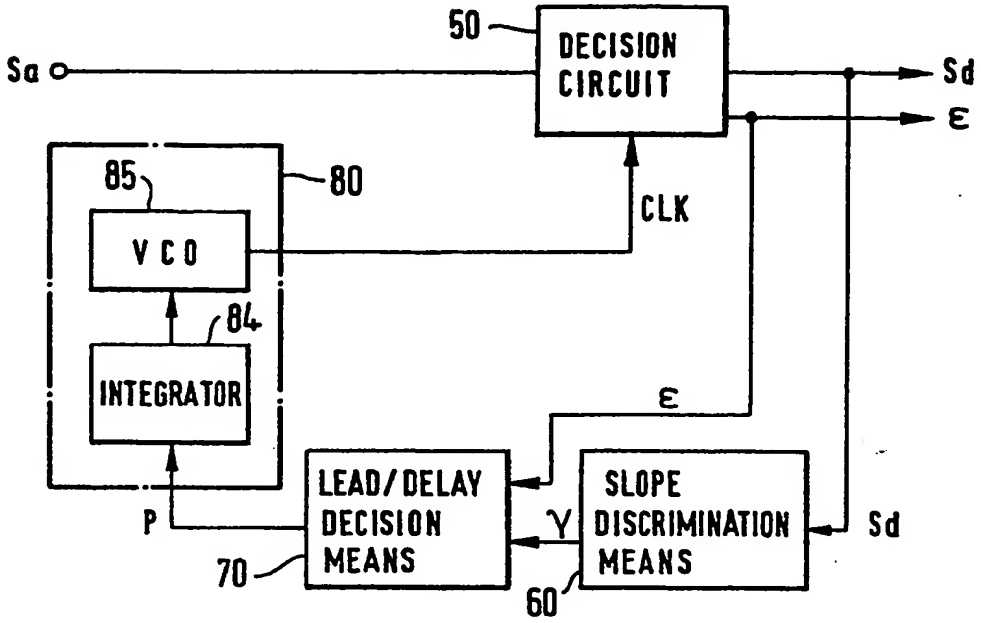


Fig.10

BASIC BLOCK DIAGRAM OF FOURTH EMBODIMENT OF PRESENT INVENTION

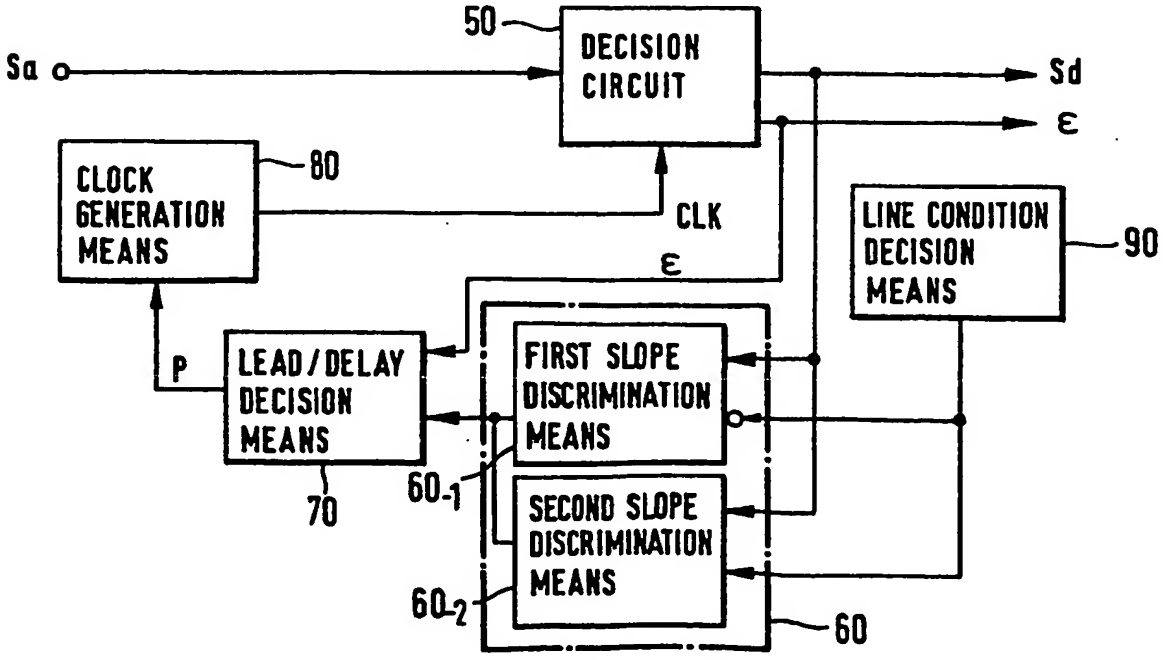
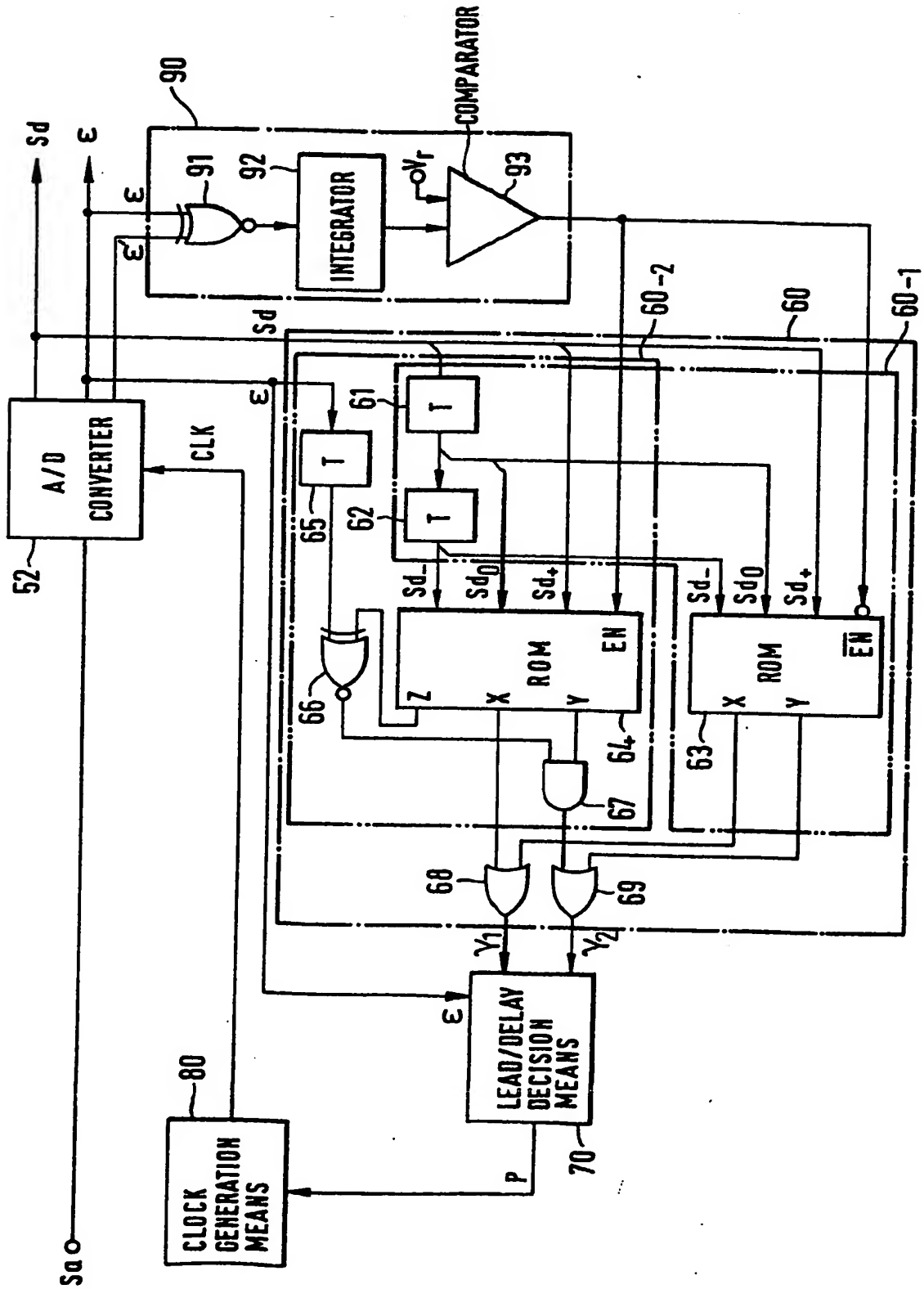


Fig. 11
DETAIL BLOCK DIAGRAM OF FOURTH EMBODIMENT OF PRESENT INVENTION



INTERNATIONAL SEARCH REPORT

0296253

International Application No PCT/JP88/00013

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl[4] H04L7/02, 25/49, 27/00

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System [5]	Classification Symbols
IPC	H04L7/02, 25/49, 27/00

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [6]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [15]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	JP, B1, 50-23926 (NEC Corporation) 12 August 1975 (12. 08. 75) P.2, left column, line 6 to p.4, right column, line 42, & US, A, 3755736	1-7
Y	JP, A, 50-81004 (International Business Machines Corp.) 1 July 1975 (01. 07. 75) P.3, upper left column, line 6 to p.6, upper right column, line 17, & DE, A, 2443870	1-7
Y	JP, A, 54-102855 (Nippon Telegraph & Telephone Public Corporation) 13 August 1979 (13. 08. 79) P.2, upper right column, line 1 to p.3, upper right column, line 19 (Family: none)	1-7
Y	JP, A, 57-142051 (Hitachi, Ltd.) 2 September 1982 (02. 09. 82) P.1, lower right column, line 18 to	1-7

* Special categories of cited documents: [19]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
March 10, 1988 (10.03.88)	March 28, 1988 (28.03.88)
International Searching Authority [1]	**Signature of Authorized Officer [20]**
Japanese Patent Office	

Form PCT/ISA/210 (second sheet) (October 1977)

International Application No PCT/JP88/00013

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

	p.2, lower right column, line 20, & US, A, 4435825	
Y	JP, A, 57-202164 (Western Electric Company, Inc.) 10 December 1982 (10. 12. 82) P.3, lower right column, line 11 to p.7, upper left column, line 14, & US, A, 4376309	1-7
Y	JP, A, 59-161149 (NEC Corporation) 11 September 1984 (11. 09. 84) P.2, upper left column, line 18 to	1-7

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE[10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers..... because they relate to subject matter [11] not required to be searched by this Authority, namely:

2. ☐ Claim numbers..... because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [12], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING[13]

This International Searching Authority found multiple inventions in this international application as follows

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest

☐ No protest accompanied the payment of additional search fees

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

	P.3, lower right column, line 9, & US, A, 4528512	
Y	JP, A, 60-251742 (NEC Corporation) 12 December 1985 (12. 12. 85) P.3, lower right column, line 6 to p.6, upper left column, line 18 (Family: none)	1-7

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE[10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers....., because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers....., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING[11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.